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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,624	02/20/2002	Jason L. Fuller	108298636US	1950
25096	7590	07/06/2004	EXAMINER	
PERKINS COIE LLP PATENT-SEA P.O. BOX 1247 SEATTLE, WA 98111-1247			HARAN, JOHN T	
		ART UNIT	PAPER NUMBER	
		1733		

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/081,624	FULLER ET AL.	
	Examiner John T. Haran	Art Unit 1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 19 April 2004.
- 2a) This action is **FINAL**.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,2,4,6-11,13,15-17,19,21,23-25,27-30 and 36-40 is/are pending in the application.
- 4a) Of the above claim(s) 3,5,12,14,18,20,22,24,26,31-35 and 41-45 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,2,4,6-11,13,15-17,19,21,23-25,27-30 and 36-40 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 20 February 2002 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date 10/10/02, 4/19/04.
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of Group I, Species Aii in the reply filed on 4/19/04 is acknowledged. It is noted that claims 22 and 32-35 were indicated as being generic. However claim 22 is directed to reflowing the preparation material which belongs in nonelected species Ai since solder is reflowed but adhesive underfill is not. Also claims 32-35 depend from claim 31 which belongs to nonelected species Ai. Accordingly claims 22 and 32-35 are withdrawn as being drawn to nonelected species Ai.

### ***Information Disclosure Statement***

2. The information disclosure statements (IDS) submitted on 10/10/02 and 4/19/04 have been considered by the examiner.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, 7-9, 10, 11, 16, 17, 23, and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Lim et al (U.S. Patent 6,378,200), Tandy (U.S. Patent 6,212,767), and Leonard (U.S. Patent 6,071,371).

The admitted prior art is directed to a method for assembling microelectronic dies wherein a flip chip die is mounted on a substrate with a first die attach machine; then the flip chip/substrate subassembly is heated to reflow solder bumps to attach the flip chip to the substrate; then flip chip/substrate subassembly is transported to a second die attach machine for dispensing epoxy on the backside of the flip chip and mounting a wire bond chip to the epoxy; and then heating the stacked die assembly to cure the epoxy (Specification 0005) Additionally the process can be performed by using a single die attach machine and running the substrate through it twice, once to attach the flip chip and once to attach the wire bond chip (Specification 0006). The admitted prior art is silent towards using a single heating cycle to secure both the flip chip to the substrate and the wire bond chip to the flip chip and towards having a single die attach machine with first and second die attach heads wherein the substrate is moved from one die attach head to another.

It is generally well known and conventional in the assembly art when assembling a plurality of chips to a substrate to have a single die attach machine with a plurality of stations, each station with its own die attach head (pick and place tool), wherein at each station particular types of chips are applied to the substrate, the substrate is moved to the next station where different types of chips are applied to the substrate and after all the chips are mounted on the substrate, the substrate is moved to a heating means for heating the attachment means between the chips and substrates to securely attach the chips to the substrate, as shown for example in Lim et al (See Figure 1; Column 2, line 39 to Column 3, line 50). One skilled in the art would have readily appreciated the

advantages of such a system over the method of the admitted prior art because it avoids having a plurality of separate die attach machines or running the substrate through the same die attach machine multiple times and provides for one heating step rather than multiple thereby increasing the efficiency as further evidenced by Tandy and Leonard et al.

Tandy is directed to a method of assembling a stacked die package wherein a first die is attached to a support substrate via a heat curable adhesive in a die attach machine containing a first die attach head and then a second die is mounted on top of the first die with a heat curable adhesive via a pick and place device (second die attach head) (See Figure 11; Column 3, lines 13-18, line 45-46, and lines 56-57). Tandy teaches that this method is preferable because it only uses one die attach machine and eliminates the need to the support substrate through a die attach machine twice, once to attach the first die and once to attach the second die (Column 1, lines 21-26). While the language of Tandy appears to teach the pick and place tool (second die attach head) is separate from the die attach machine (with the first die attach head), Tandy is essentially teaching a single machine (or system) that has two separate die attach heads (or devices).

Leonard et al is directed towards a method for bonding two dies to a circuit board, one via solder and the other via curable adhesive and teaches that it is preferable to perform one heating cycle to both reflow the solder and cure the adhesive rather than two separate heating cycles, one for the solder and one for the adhesive,

because the additional heating has detrimental effects and is inefficient (Column 1, line 40 to Column 2, line 40).

One skilled in the art would have readily appreciated that the collective teachings of Lim et al, Tandy, and Leonard et al point out the inefficiencies of the admitted prior art and suggest modifying the method of the admitted prior art to have a single die attach machine with two die attach stations, each with its own die attach head, wherein the flip chip is mounted on the substrate at the first station by a first die attach head, is transported directly to a second station wherein the wire bond chip is mounted on the flip chip by a second die attach head and then the entire assembly is transported to a heating means for heating the solder and adhesive simultaneously in a single heating cycle to attach the flip chip to the substrate and the wire bond chip to the flip chip. Such a method would have increased efficiency and productivity as suggested in Lim et al, Tandy, and Leonard et al.

Regarding claims 1, 2, 7-9, 10, 11, 16, 17, 23, and 27-30, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of the admitted prior art as suggested above by the collective teachings of Lim et al, Tandy, and Leonard et al in order to increase the efficiency and productivity of the admitted prior art.

5. Claims 4, 13, 19, 25, 36 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Lim et al (U.S. Patent 6,378,200), Tandy (U.S. Patent 6,212,767), and Leonard (U.S. Patent 6,071,371) as applied to

claims 1, 2, 7-9, 10, 11, 16, 17, 23, and 27-30 above, and further in view of Imasu et al (U.S. Patent 6,208,525).

The admitted prior art is silent towards applying an adhesive underfill to the substrate, placing the flip chip on the adhesive and curing the adhesive to attach the flip chip to the substrate, however such is well known and conventional in the flip chip art, as shown for example in Imasu et al (See Figures 5-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use conventional means for adhering the flip chip to the substrate in the method of the admitted prior art, as modified above.

6. Claims 6, 15, 21, 27, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Lim et al (U.S. Patent 6,378,200), Tandy (U.S. Patent 6,212,767), and Leonard (U.S. Patent 6,071,371) as applied to claims 1, 2, 7-9, 10, 11, 16, 17, 23, and 27-30 above, and further in view of Takiar et al (U.S. Patent 5,422,435)

The admitted prior art is silent towards having a third chip bonded to the top of the wire bond chip, however it is well known and conventional in the art to have a stack of three chips adhered to each other via adhesive, as shown for example in Takiar et al (See Figures 3 and 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to bond a third chip to the top of the wire bond chip in the method of the admitted prior art, as modified above, as is conventional in the art and to do so in a manner that the third chip is attached in the same die bonding machine

and the adhesive is cured at the same time as the others for the same reasons of efficiency and productivity noted above.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US2003/0145939 is cited for teaching many of the same "inventive" concepts as the present applicant, but it is not available as prior art.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John T. Haran** whose telephone number is **(571) 272-1217**. The examiner can normally be reached on M-Th (8 - 5) and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Blaine Copenheaver can be reached on (571) 272-1156. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*John T. Haran*  
John T. Haran  
Examiner  
Art Unit 1733